IN THE CLAIMS:

Please amend the pending claims as follows:

1. (Currently Amended) A computer system comprising:

a processor having an external input, ~~and responsive to a signal at said input, reducing a~~ such that said processor is to reduce power consumption of said processor by reducing a frequency of an internal clock of the processor if a signal at said external input is asserted; and

a power reduction circuit coupled to said input of said processor and providing [[a]] an output signal to said input of said processor in response to a failure condition affecting said processor such that the power consumption of said processor is periodically reduced based on said output signal.

2. (Original) A computer system according to claim 1, wherein a first signal level of the signal at the input of the processor stops an internal clock of the processor.

3. (Original) A computer system according to claim 1, wherein said signal provided to said input of said processor in response to said failure condition comprises a periodic signal including at least a first signal level and a second signal level.

4. (Original) A computer system according to claim 1, further comprising a cooling fan directing air toward said processor, wherein said failure condition affecting said processor corresponds to a reduced performance of said cooling fan.

5. (Original) A computer system according to claim 4, said power reduction circuit including a signal generator generating said periodic signal.

6. (Original) A computer system according to claim 5, wherein said signal generator includes inputs corresponding to characteristics of said generated periodic signal.

7. (Original) A computer system according to claim 5, wherein said signal generator includes an input corresponding to a duty cycle of said generated periodic signal and an input corresponding to a frequency or a period of said generated periodic signal.

8. (Original) A computer system according to claim 1, wherein said power reduction circuit detects a temperature of said processor, wherein said failure condition affecting said processor is detected when said detected temperature of said processor is above a predetermined temperature.

9. (Original) A computer system according to claim 1, wherein said power reduction circuit includes a sensor detecting a temperature of said processor, wherein said failure condition affecting said processor is detected when said sensed temperature of said processor is above a predetermined temperature.

10. (Original) A computer system according to claim 9, wherein said sensor comprises a temperature sensor embedded in a heat sink attached to said processor.

11. (Original) A computer system according to claim 3, said power reduction circuit including a switch providing said periodic signal to said input in response to a presence of said failure condition affecting said processor, said switch providing said second signal level to said input in response to an absence of said failure condition affecting said processor.

12. (Original) A computer system according to claim 3, said power reduction circuit including a multiplexor providing said periodic signal to said input in response to a presence of said failure condition affecting said processor, said multiplexor providing said second signal level to said input in response to an absence of said failure condition affecting said processor.

13. (Original) A computer system according to claim 1, wherein said failure condition affecting said processor is a thermal temperature condition corresponding to an overtemperature condition of said processor at or near said processor.

14. (Original) A computer system according to claim 1, said computer system further comprising:

at least one additional processor each having an input, wherein a power consumption of each processor is reduced in response to a first signal level of the input of that processor and is not reduced in response to a second signal level of the input of that processor; and

at least one additional power reduction circuit, each said additional power reduction circuit respectively corresponding to each said at least one additional processor and providing a signal to said input of said corresponding processor in response to a failure condition affecting the

corresponding processor, wherein said signal provided to said input of said corresponding processor comprises a periodic signal including at least the first signal level and the second signal level.

15. (Currently Amended) An apparatus for reducing a power consumption of a processor, comprising:

a signal generator ~~generating~~ to generate a failure condition signal indicating a failure condition affecting said processor; and

a power reduction circuit responsive to said failure condition signal and providing a periodic signal ~~for~~ to periodically ~~reducing a~~ reduce power consumption of said processor, said processor including an external input such that said processor is adapted to reduce power consumption by reducing a frequency of an internal clock of said processor when a signal at said external input is asserted.

16. (Original) An apparatus according to claim 15, wherein said apparatus includes said processor, and said processor has a power consumption reduction input, wherein said power reduction circuit provides said periodic signal to said power consumption reduction input of said processor in response to said failure condition signal.

17. (Original) An apparatus according to claim 16, wherein an internal clock of the processor is stopped in response to the power consumption reduction input of the processor.

18. (Original) An apparatus according to claim 15, further comprising a cooling fan directing air toward said processor, wherein said failure condition affecting said processor corresponds to a reduced performance of said cooling fan.

19. (Original) An apparatus system according to claim 15, said power reduction circuit including a signal generator generating said periodic signal.

20. (Original) An apparatus according to claim 15, wherein said power reduction circuit includes a sensor detecting a temperature of said processor, wherein said failure condition affecting said processor is detected when said sensed temperature of said processor is above a predetermined temperature.

21. (Original) An apparatus according to claim 20, wherein said sensor comprises a temperature sensor embedded in a heat sink attached to said processor.

22. (Original) An apparatus according to claim 16, said power reduction circuit including a switch providing said periodic signal to said power consumption reduction input in response to a presence of said failure condition affecting said processor.

23. (Original) An apparatus according to claim 16, said power reduction circuit including a multiplexor providing said periodic signal to said power consumption reduction input in response to a presence of said failure condition affecting said processor.

24. (Currently Amended) An apparatus according to claim 15, wherein said failure condition affecting said processor is a [[a]] thermal failure condition corresponding to an overtemperature condition of said processor at or near said processor.

25. (Currently Amended) A method of reducing a power consumption of a processor, comprising ~~steps of~~:

detecting a failure condition affecting said processor; and

periodically reducing a power consumption of said processor in response to said ~~step of~~ detecting said failure condition by generating a periodic signal and supplying it to an external input to the processor, such that said processor is to reduce power consumption by reducing a frequency of an internal clock of said processor if a signal at said external input is asserted.

26. (Original) A method according to claim 25, wherein said step of periodically reducing the power consumption of said processor comprises periodically stopping an internal clock of said processor.

27. (Original) A method according to claim 25, further comprising a step of measuring a temperature at or near said processor and providing said signal indicating a failure condition affecting said processor in response to said measured temperature.

28. (Original) A method according to claim 25, further comprising a step of providing said signal indicating a failure condition affecting said processor in response to a reduction in performance of a cooling fan.

29. (Original) A method according to claim 25, wherein said failure condition affecting said processor corresponds to an overtemperature condition of said processor at or near said processor.

30. (Original) A method according to claim 25, wherein said failure condition affecting said processor is a thermal failure condition affecting a temperature of said processor.